JAMIA HAMDARD
Department of Computer Science & Engineering
School of Engineering Sciences & Technology
New Delhi-110062

Examination: Odd Semester Examination 2023

Paper Name: Digital Electronics **Paper Code: BTECE 305**
Time: 3 Hours **Maximum Marks: 75**

Section A

Note: Attempt ALL the questions 7x5=35

Q. No.	Question	Marks	CO	BL
1.	i) Convert $(1001.1001)_2$ to its octal equivalent. ii) Explain the importance of Karnaugh maps in digital logic gate implementation.	5	CO1	1, 2, 3
2.	Explain the working of low-level and high-level triggered S-R Latch with the help of the logic level diagram.	5	CO3	1, 2, 3
3.	Explain the importance of different digital performance parameters such as Noise margin, Propagation delay, and fan-out.	5	CO4	1, 2, 3
4.	Design a 2-bit Comparator with the help of universal gates and discuss its working in brief.	5	CO2	2, 3, 4, 5
5.	Differentiate between SOP & POS forms of logic gate implementation with the help of examples.	5	CO1	1, 2, 3
6.	Write a Behavioural modelling style VHDL program for implementing 4:1 Multiplexer.	5	CO5	1, 2, 3
7.	Discuss the read and write operation of DRAM cell with the help of timing diagram.	5	CO4	1, 2, 3

Section B

Note: Attempt any FOUR (4) Questions **(4x10=40)**

Q. No.	Question	Marks	CO	BL
1.	Design a 4-bit binary parallel adder using 1-bit full adder, and explain its working in detail.	10	CO2	2, 3, 4, 5, 6
2.	Design a Pseudo Random Binary Sequence generator using different logic blocks and explain its working in details.	10	CO3	2, 3, 4, 5, 6
3.	i) Explain the working and advantages of Master-Slave JK FF over the other Flip Flops. ii) Design a Mod 8 asynchronous counter using D Flipflop.	10	CO3	2, 3, 4, 5

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4.	Explain the different style of VHDL modelling in detail with the help of examples in terms of its requirement and advantages.	**10**	**CO5**	**1, 2, 3**
5.	Explain the importance of converting one form of number into a another. And also design an Excess-3 code converter with help of Basic logic gates.	**10**	**CO1**	**1, 2, 3, 4, 5**
6.	Explain any TWO of the following: a) Tristate TTL c) CMOS families d) FPGA e) ALU	**10**	**CO4, CO5**	**1, 2**

BL : Bloom's Taxonomy Level (1-Remembering, 2-Understanding, 3-Applying, 4- Analysing, 5-Evaluating, 6- Creating)