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Odd Semester Examination 2024

Paper Name: Digital System Design **Paper Code: BTECE 305**
Time: 2 Hours 30 Minutes **Maximum Marks: 60**

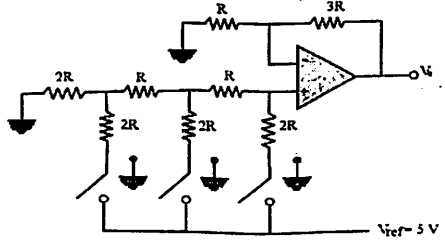
Section A

Note: Attempt ALL the questions **4x5=20**

Q. No.	Question	CO	BL
1.	Simplify following using K-Map. i) $F(A, B, C, D) = \Sigma m(0, 1, 2, 5, 7, 8, 9, 10, 13, 15)$ ii) $F(A, B, C, D) = \Sigma m(1, 3, 4, 6, 8, 9, 11, 13, 15) + \Sigma d(0, 2, 14)$	CO2	2
2.	Explain the design and working of an active high and active low SR Flipflop	CO4	4
3.	Construct 4 bit parallel full subtractor using full adders.	CO3	5
4.	Explain the working of 1x8 DEMUX. Derive its circuit diagram and expression.	CO3	4

Section B

Note: Attempt any FOUR (4) Questions **(4x10=40)**

Q. No.	Question	CO	BL
1.	Explain the working of an R-2R ladder type DAC. In the circuit given below Solve for V_0 if R = 10 KΩ, with binary input 010. 	CO5	3
2.	Construct JK flip flop using T flip flop. Also explain the cause of the race around condition in JK flipflop and suggest the methods to remove it.	CO4	5
3.	Differentiate between synchronous counter and an asynchronous counter. Design a Mod 6 synchronous counter using T Flipflop.	CO4	5
4.	Write a VHDL program using behavioural architecture for the implementation of Full Adder.	CO5	4
5.	Construct 8:1 MUX using 2:1 MUX. What is the significance of select lines in a multiplexer, explain with the help of examples.	CO2	5
6.	Convert the following: i) $(365.7)_8 = (?)_{10}$ ii) $(85642.77)_{10} = (?)_2$ iii) $(101101100100.011)_2 = (?)_{16}$ iv) $(ABD.EE)_{16} = (?)_8$	CO1	2

BL : Bloom's Taxonomy Level (1-Remembering, 2-Understanding, 3-Applying, 4- Analysing, 5-Evaluating, 6- Creating)