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Odd Semester Examination-2024

Paper Name: Computer System Architecture **Paper Code: BCA 102/ BSC-102**

Total Marks: 60 **Total Time: $2\frac{1}{2}$ Hrs.**

[SECTION-A]
All questions are compulsory
***Mark-True or False* [20 Marks]**

Q. No.	Questions	Marks	CO	BL
1.	NAND and NOR gates are considered universal gates because all other gates can be derived from them.	1	CO1	L 2
2.	Boolean expressions can always be minimized to a single literal variable.	1	CO1	L5
3.	In sequential circuits, the current state and input determine the next state.	1	CO1	L2
4.	Designing a counter using flip-flops involves both combinational and sequential logic concepts.	1	CO1	L3
5.	The performance of a multiplexer is unaffected by the number of select lines.	1	CO1	L5
6.	The floating-point standard IEEE 754 ensures that all decimal numbers can be exactly represented.	1	CO2	L4
7.	In base-8 (octal) representation, each digit corresponds to exactly three binary bits.	1	CO2	L2
8.	Designing a system that directly converts between binary and Gray code involves reducing multi-step mapping.	1	CO2	L6
9.	In fixed-point representation, the position of the decimal point must be defined externally.	1	CO2	L1
10.	Evaluating large integer multiplications in computers is often less efficient than floating-point operations.	1	CO2	L5
11.	A basic computer's timing and control signals are solely determined by the instruction set design.	1	CO3	L4
12.	Interrupt service routines (ISRs) prioritize critical processes while suspending less urgent tasks.	1	CO3	L3
13.	Address decoding in a basic computer design helps evaluate and locate specific components in memory.	1	CO3	L6
14.	Developing a more complex instruction set enhances execution time for simple computational tasks.	1	CO3	L5
15.	Interconnection structures like buses in computer architecture provide parallel access paths to I/O devices.	1	CO3	L4

16.	Micro programmed control requires rewriting the control words in the ROM when modifying system operations.	1	CO4	L5
17.	Pipelining improves instruction throughput by reducing total instruction execution time.	1	CO4	L4
18.	Evaluating the trade-offs between stack-based and accumulator-based CPU organizations helps optimize system performance.	1	CO4	L5
19.	The simplicity of instruction decoding in RISC processors makes them less suited for multitasking systems.	1	CO4	L6
20.	A multi-level cache system with dynamic cache replacement policies could enhance performance by adjusting to varying access patterns.	1	CO4	L2

[SECTION-B]

Attempt any FOUR questions. **[20 Marks]**

Q. No.	Questions	Marks	CO	BL
1.	Explain the working principle of flip-flops and discuss the different types ***(SR, JK, D, and T)***. Briefly describe their applications in sequential circuits and how a flip-flop can be used to implement a 2-bit counter.	5	CO1 and CO2	L2 and L3
2.	What is the difference between serial and parallel data transfer? Using a shift register with parallel load, explain briefly how to convert serial input data to parallel output and parallel input data to serial output."	5	CO1 and CO2	L2 and L3
3.	Explain how to convert a binary number to its hexadecimal equivalent. Demonstrate the conversion process for the following binary numbers: **(a)** 110110110101 **(b)** 1010011101011010	5	CO1 and CO3	L2 and L3
4.	Describe three types of instruction formats used in CPUs. Highlight their key differences, provide examples of their use, and explain how each affects processor performance and complexity.	5	CO1 and CO2	L2 and L4
5.	Explain the key differences between RISC (Reduced Instruction Set Computer) and CISC (Complex Instruction Set Computer) architectures. Highlight the advantages and disadvantages of each approach in terms of execution speed, memory usage, and ease of implementation.	5	CO1 and CO2	L2 and L4
6.	What is the difference between RAM and ROM? What function does each serve in a microcomputer system? How many 128 × 8 RAM chips are needed to provide a memory capacity of 2048 bytes?	5	CO1	L1

[Section-C]

Attempt any TWO questions. [20 Marks]

Q. No.	Questions	Marks	CO	BL
1.	Describe the need for addressing in a computer system and its significance in program execution. Explain the various addressing modes used in computer architecture, including immediate, direct, indirect, register, and indexed modes, with suitable examples to illustrate their functionality and applications."	10	CO1	L 2
2.	Describe the working mechanism of a Direct-Mapped Cache. A digital computer has a memory unit of 64K × 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of four words. Answer the following: **(a)** How many bits are there in the tag, index, block, and word fields of the address format? **(b)** How many bits are there in each word of the cache, and how are they divided into functions? Include a valid bit in your explanation. **(c)** How many blocks can the cache accommodate?"	10	CO1 and CO2	L 2 and L 3
3.	Discuss Flynn's Classification (SISD, SIMD, MISD, and MIMD) and its significance in modern computer architectures. Evaluate how each category impacts parallel processing, processor design, and computational efficiency with examples.	10	CO5	L 4
4.	Design a BCD to Seven-Segment Decoder circuit and explain its theoretical and practical applications. Your answer should include: **(a)** A truth table for BCD inputs ***(0000 to 1001),*** listing the corresponding outputs for each segment ***(a to g)*** of the seven-segment display. **(b)** Derivation of simplified Boolean expressions for each output segment ***(a, b, c, d, e, f, g)*** based on the truth table. **(c)** A logic circuit diagram using appropriate logic gates ***(AND, OR, NOT)*** to implement the BCD to seven-segment decoder. **(d)** A discussion of at least three real-life applications of BCD to Seven-Segment Decoders.	10	CO3 and CO4	L3 and L6

BL- Bloom's taxonomy Level: (1- Remembering, 2-Understanding, 3-Applying, 4-Analyzing, 5-Evaluating, 6-Creating)