ROLL NO._____ ENROLLMENT NO._____

DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING, SCHOOL OF ENGINEERING SCIENCES & TECHNOLOGY, JAMIA HAMDARD

EVEN SEMESTER EXAMINATION 2023

BTCSE 402/BTCSEAI 402

COMPUTER ORGANIZATION AND ARCHITECTURE

TIME: 3 HRS **MAXIMUM MARKS:75**

Note: Do not write anything on paper except Roll No. & Enrollment No. Use of mobile phone is not allowed. Please follow proper numbering while answering the questions Proper steps are required to be specified for all questions

SECTION A

All questions of Section A are compulsory (7*5)

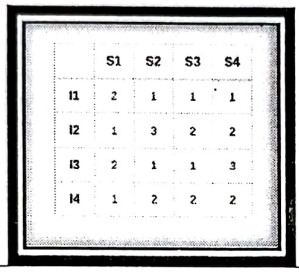
S(●)	QUESTIONS	MARKS	CO	BL
Q1.	Consider a fully associative mapped cache of size 512 KB with block size 1 KB. There are 17 bits in the tag. Find- Size of main memory and Tag directory size.	5	CO2	L3
Q2.	Which addressing modes are most appropriate match for the following (explanations are must): Array implementation, writing relocatable code, Passing array as parameter, Loops, Pointers and Constants	5	CO3	L2
Q3.	The simplest way to examine the advantages and disadvantages of RISC architecture is by contrasting it with its predecessor: CISC (Complex Instruction Set Computers) architecture. Do the needful.	5	CO2	L1
Q4.	Through real world examples provide details of Computer Architecture, Computer Organization and DMA.	5	CO1	L4
Q5.	Instruction execution in a processor is divided into 5 stages, Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Execute (EX), and Write Back (WB). These stages take 5, 4, 20, 10 and 3 nanoseconds (ns) respectively. A pipelined implementation of the processor requires buffering between each pair of consecutive stages with a delay of 2 ns. Two pipelined implementations of the processor are contemplated: (i) a naive pipeline implementation (NP) with 5 stages and (ii) an efficient pipeline (EP) where the OF stage is divided into stages OF1 and OF2 with execution times of 12 ns and 8 ns respectively. The speedup (correct to two decimal places) achieved by EP over NP in executing 20 independent instructions with no hazards is?	5	C04	L5
Q6.	For the table below find the results: R1=98 and XR=3. Find the effective address and content of accumulator for Direct, Immediate, Indirect, Relative, Indexed, Register, Register direct, Register Indirect, Autodecrement and autoincrement addressing modes.	5	CO5	L6

50	Load to Ac Mode
51	Address= 100
52	Next Instruction
97	450
98	700
99	800
100	105
101	35
102	45
103	65
104	75
105	500
152	70

Q7.	Using Booth's Algorithm for multiplication, the multiplier -57 will be recoded as? Through a flowchart specify process for the same process.	5	CO4	L3

SECTION B

Answer any 4 questions in Section B (4*10)

S.NO	QUESTIONS	MARKS	CO	BL
Q1.	Consider a 4 stage pipeline processor. The number of cycles needed by the four instructions I1, I2, I3 and I4 in stages S1, S2, S3 and S4 is shown below- What is the number of cycles needed to execute the following loop? for(i=1 to 2) { I1; I2; I3; I4; } 	10	CO3	L2
Q2.	Suppose for a process P, reference to pages in order are 1,2,4,5,2,1,2,4. Assume that main memory can accommodate 2 pages and the main memory has already 1 and 2 in the order, 1– first, 2– second. At this moment, assume LFU and LRU Page Replacement Algorithm, then find the number of page faults that occur to complete the execution of process of both algorithms.	10	CO3	L3
Q3.	Consider a 4-way set associative cache (initially empty) with total 16 cache blocks. The main memory consists of 256 blocks and the request for memory blocks is in the following order: 0, 255, 1, 4, 3, 8, 133, 159, 216, 129, 63, 8, 48, 32, 73, 92, 155. Which memory block will NOT be in cache if LRU replacement policy is used?	10	CO1	L1
Q4.	Find MAL. Time ⟶ 1 2 3 4 5 S_1 X X S_2 X X S_3 X	10	CO4	L4
Q5.	For multiplier 001100 and multiplicand 010011 find the booth multiplication result.	10	CO5	L5
Q6.	Consider a 8-way set associative mapped cache with block size 4 KB. The size of main memory is 16 GB and there are 10 bits in the tag. Find- Size of cache memory and tag directory size.	10	CO2	L6

BLOOMS TAXANOMY LEVELS (BL)
1-REMEMBERING, 2-UNDERSTANDING, 3-APPLYING, 4-ANALYSING,
5-EVALUATING, 6-CREATING