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Examination: Even Semester Examination 2023

Paper Name: Design and Analysis of VLSI Subsystem **Paper Code: BTECE MOOCS1**
Time: 3 Hours **Maximum Marks: 75**

Section A

Note: Attempt ALL the questions 7x5=35

Q. No.	Question	Marks	CO	BL
1.	Explain the working of an NMOS transistor.	5	CO1	3
2.	What is a skew inverter? With the help of an example define Hi Skew, Low Skew and Unskewed inverter.	5	CO2	1
3.	Explain the Evolution of IC technologies	5	CO3	5
4.	Explain CMOS Lambda based design rules	5	CO1	5
5.	Explain stage ratio for larger load	5	CO3	6
6.	Design a 2:1 multiplexer using tristate logic families.	5	CO4	6
7.	How survivability of a system is important in VLSI design?	5	CO5	4

Section B

Note: Attempt any FOUR (4) Questions (4x10=40)

Q. No.	Question	Marks	CO	BL
1.	Explain subthreshold leakage current model.	10	CO1	3
2.	Design the layout (stick diagram) of 1-bit adder.	10	CO2	4
3.	Describe the working of a basic CMOS SR latch using 2 input NAND gate	10	CO3	2
4.	Explain the process of CMOS fabrication	10	CO4	2
5.	Explain the design of an ALU subsystem.	10	CO5	6
6.	Write a short note on the following: a) Gate area (Ag) b) Parasitic Capacitance c) Scaling	10	CO3	5

BL : Bloom's Taxonomy Level (1-Remembering, 2-Understanding, 3-Applying, 4- Analysing, 5-Evaluating, 6- Creating)