ROLL NO._____ ENROLLMENT NO._____

DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING, SCHOOL OF ENGINEERING SCIENCES & TECHNOLOGY, JAMIA HAMDARD

ODD SEMESTER EXAMINATION 2024 (BACKLOG)

COMPUTER ORGANIZATION AND ARCHITECTURE (MCA 102)

TIME: 2.5 HRS **MAXIMUM MARKS:60**

Note: Do not write anything on paper except Roll No. & Enrollment No. Use of mobile phone is not allowed. Please follow proper numbering while answering the questions Proper steps are required to be specified for all questions

SECTION A

All questions of Section A are compulsory (4*5=20)

<table>
<tr><th>S.NO</th><th>QUESTIONS</th><th>MARKS</th><th>CO</th><th>BL</th></tr>
<tr><td>Q1.</td><td>What is virtual memory? Explain the steps involved in virtual memory address translation.</td><td>5</td><td>CO2</td><td>L3</td></tr>
<tr><td>Q2.</td><td>For the reservation table below find forbidden latencies, collision vector, simple and greedy cycles, and state diagram. (5)
<table>
<tr><td></td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td></tr>
<tr><td>S1</td><td>X</td><td></td><td></td><td></td><td></td><td>X</td></tr>
<tr><td>S2</td><td></td><td>X</td><td></td><td></td><td>X</td><td></td></tr>
<tr><td>S3</td><td></td><td></td><td>X</td><td></td><td></td><td></td></tr>
<tr><td>S4</td><td></td><td></td><td></td><td>X</td><td></td><td></td></tr>
<tr><td>S5</td><td>X</td><td></td><td></td><td></td><td></td><td>X</td></tr>
</table></td><td>5</td><td>CO3</td><td>L2</td></tr>
<tr><td>Q3.</td><td>Given page reference string:
• 1,2,3,4,2,1,5,6,2,1,2,3,7,6,3,2,1,2,3,6
• Compare the number of page faults for LRU and FIFO.</td><td>5</td><td>CO2</td><td>L1</td></tr>
<tr><td>Q4.</td><td>Consider a pipeline having 4 phases with duration 60, 50, 90 and 80 ns. Given latch delay is 10 ns. Calculate- Pipeline cycle time, Non-pipeline execution time, Speed up ratio, Pipeline time for 1000 tasks, Sequential time for 1000 tasks and Throughput.</td><td>5</td><td>CO1</td><td>L4</td></tr>
</table>

SECTION B

Answer any 4 questions in Section B (4*10=40)

S.NO	QUESTIONS	MARKS	CO	BL
Q1.	Consider a 2-way set associative mapping is used where there are 8 cache blocks (0 – 7). If LRU is used to replace the memory blocks then what is the number of blocks present in cache after end of the following sequence (0, 4, 9, 5, 16, 13, 15, 19, 25, 63, 24, 57, 30)?	10	CO3	L2
Q2.	What is meant by instruction pipeline? Explain four segment Instruction Pipeline. Give its timing diagram.	10	CO3	L3
Q3.	Instruction execution in a processor is divided into *5 stages, Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Execute (EX), and Write*	10	CO1	L5

	Back (WB). These stages take **5, 4, 20, 10** and **3 nanoseconds (ns)** respectively. A pipelined implementation of the processor requires buffering between each pair of consecutive stages with a delay of **2 ns**. Two pipelined implementations of the processor are contemplated: (i) a naive pipeline implementation (NP) with 5 stages and (ii) an efficient pipeline (EP) where the OF stage is divided into stages OF1 and OF2 with execution times of **12 ns** and **8 ns** respectively. The speedup (correct to two decimal places) achieved by EP over NP in executing 20 independent instructions with no hazards is?			
Q4.	For multiplier 001100 and multiplicand 010011 find the booth multiplication result.	10	CO4	L4
Q5.	Explain direct and immediate addressing Modes. Differentiate CISC and RISC processors	10	CO5	L5
Q6.	For the table below find the results: R1=98 and XR=3 Find the effective address and content of accumulator for Direct, Immediate, Indirect, Relative, Indexed, Register, Register direct, Register Indirect, Autodecrement and autoincrement addressing modes.	10	CO2	L6

50	Load to Ac Mode
51	Address= 100
52	Next Instruction
97	450
98	700
99	800
100	105
101	35
102	45
103	65
104	75
105	500
152	70

BLOOMS TAXANOMY LEVELS (BL)

1-REMEMBERING, 2-UNDERSTANDING, 3-APPLYING, 4-ANALYSING, 5-EVALUATING, 6-CREATING