JAMIA HAMDARD
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Examination: Even Semester Examination 2023

Paper Name: Digital IC Design
Paper Code: BTECE MOOCS 2/Lateral Entry
Time: 3 Hours **Maximum Marks: 75**

Section A

(7x5=35)

Note: Attempt all the questions

Q.No.	Question	Marks	BL
1.	Draw and explain the Transfer characteristics of CMOS Inverter.	5	BL1
2.	Explain the MOS Capacitor threshold voltage.	5	BL2
3.	Explain and differentiate Latch and Flip Flop?	5	BL4
4.	What is the difference between combinational and sequential logic circuits?	5	BL1
5.	Explain the parasitic Delay in CMOS.	5	BL1
6.	What do you understand by Gate sizing and Buffering	5	BL3
7.	Explain the Mirror Adder.	5	BL2

Section B

Note: Attempt any <u>four (4)</u> Questions **(4x10=40)**

Q.No.	Question	Marks	BL
1.	Draw and explain the working of CMOS NAND gate .	**10**	**BL2**
2.	Explain the process steps in the fabrication of an integrated circuit.	**10**	**BL2**
3.	Draw and explain the full adder in detail.	**10**	**BL2**
4.	Explain about setup time and hold time, what will happen if there is setup time and hold tine violation, how to overcome this?	**10**	**BL4**
5.	Discuss and explain digital circuit design and challenges and opportunities in the era of nanoscale CMOS.	**10**	**BL1**
6.	Write a short note on any two of the followings: a. Carry save multiplier b. D flipflop c. Transition capacitance d. Stacking Effect	**5x2=10**	**BL2**