

ROLL NO. _____

ENROLLMENT NO. _____

**DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING, SCHOOL OF ENGINEERING SCIENCES
& TECHNOLOGY, JAMIA IAMDARD**

SUPPLEMENTARY EXAMINATION 2023

BTCSE 402/BTCSEAI 402 COMPUTER ORGANIZATION AND ARCHITECTURE
TIME: 3 HRS **MAXIMUM MARKS:75**

Note: Do not write anything on paper except Roll No. & Enrollment No. Use of mobile phone is not allowed. Please follow proper numbering while answering the questions Proper steps are required to be specified for all questions

SECTION A

*All questions of Section A are compulsory (7*5)*

S.NO	QUESTIONS	MARKS	CO	BL																																							
Q1.	Consider a fully associative mapped cache of size 1024 KB with block size 1 KB. There are 20 bits in the tag. Find- Size of main memory and Tag directory size.	5	CO2	L3																																							
Q2.	Draw diagrammatic representation of the addressing modes that are most appropriate match for the following (explanations are must): Array implementation, writing relocatable code, Passing array as parameter, Loops, Pointers and Constants	5	CO3	L2																																							
Q3.	The simplest way to examine the advantages and disadvantages of RISC architecture is by contrasting it with its predecessor: CISC (Complex Instruction Set Computers) architecture. Do the needful.	5	CO2	L1																																							
Q4.	Differentiate Computer Architecture and Computer Organization?	5	CO1	L4																																							
Q5.	Explain Von Neumann and Harvard architecture with suitable diagrams. Illustrate with diagrams the various components and it's functioning (or) With a neat sketch, explain in detail about the functional units of computers.	5	CO4	L5																																							
Q6.	For the table below find the results: <table><tr><td>50</td><td>Load to Ac</td><td>Mode</td></tr><tr><td>51</td><td>Address= 200</td><td></td></tr><tr><td>52</td><td>Next Instruction</td><td></td></tr><tr><td>97</td><td>400</td><td></td></tr><tr><td>98</td><td>700</td><td></td></tr><tr><td>99</td><td>800</td><td></td></tr><tr><td>100</td><td>105</td><td></td></tr><tr><td>101</td><td>35</td><td></td></tr><tr><td>102</td><td>45</td><td></td></tr><tr><td>103</td><td>65</td><td></td></tr><tr><td>104</td><td>75</td><td></td></tr><tr><td>105</td><td>500</td><td></td></tr><tr><td>152</td><td>70</td><td></td></tr></table> R1=100 and XR=5. Find the effective address and content of accumulator for Direct, Immediate, Indirect, Relative, Indexed, Register, Register direct, Register Indirect, Autodecrement and autoincrement addressing modes.	50	Load to Ac	Mode	51	Address= 200		52	Next Instruction		97	400		98	700		99	800		100	105		101	35		102	45		103	65		104	75		105	500		152	70		5	CO5	L6
50	Load to Ac	Mode																																									
51	Address= 200																																										
52	Next Instruction																																										
97	400																																										
98	700																																										
99	800																																										
100	105																																										
101	35																																										
102	45																																										
103	65																																										
104	75																																										
105	500																																										
152	70																																										
Q7.	Explain Booth's Algorithm through a flowchart?	5	CO4	L3																																							

SECTION B
Answer any 4 questions in Section B (4*10)

S.NO	QUESTIONS	MARKS	CO	BL																									
Q1.	Consider a 4 stage pipeline processor. The number of cycles needed by the four instructions I1, I2, I3 and I4 in stages S1, S2, S3 and S4 is shown below- What is the number of cycles needed to execute the following loop? for(i=1 to 2) { I1; I2; I3; I4; } <table><tr><td></td><td>S1</td><td>S2</td><td>S3</td><td>S4</td></tr><tr><td>I1</td><td>2</td><td>1</td><td>1</td><td>1</td></tr><tr><td>I2</td><td>1</td><td>3</td><td>2</td><td>2</td></tr><tr><td>I3</td><td>2</td><td>1</td><td>1</td><td>3</td></tr><tr><td>I4</td><td>1</td><td>2</td><td>2</td><td>2</td></tr></table>		S1	S2	S3	S4	I1	2	1	1	1	I2	1	3	2	2	I3	2	1	1	3	I4	1	2	2	2	10	CO3	L2
	S1	S2	S3	S4																									
I1	2	1	1	1																									
I2	1	3	2	2																									
I3	2	1	1	3																									
I4	1	2	2	2																									
Q2.	Define pipeline processing. Explain pipeline hazards?	10	CO3	L3																									
Q3.	Consider a 4-way set associative cache (initially empty) with total 16 cache blocks. The main memory consists of 256 blocks and the request for memory blocks is in the following order: 0, 255, 1, 4, 3, 8, 133, 159, 216, 129, 63, 8, 48, 32, 73, 92, 155. Which memory block will NOT be in cache if LRU replacement policy is used?	10	CO1	L1																									
Q4.	Find greedy cycles for the reservation table mentioned below: Time → <table><tr><td></td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td></tr><tr><td>S₁</td><td>X</td><td></td><td></td><td></td><td>X</td></tr><tr><td>S₂</td><td></td><td>X</td><td></td><td>X</td><td></td></tr><tr><td>S₃</td><td></td><td></td><td>X</td><td></td><td></td></tr></table>		1	2	3	4	5	S ₁	X				X	S ₂		X		X		S ₃			X			10	CO4	L4	
	1	2	3	4	5																								
S ₁	X				X																								
S ₂		X		X																									
S ₃			X																										
Q5.	For multiplier 1100 and multiplicand 0011 find the booth multiplication result.	10	CO5	L5																									
Q6.	Consider a 8-way set associative mapped cache with block size 4 KB. The size of main memory is 16 GB and there are 10 bits in the tag. Find- Size of cache memory and tag directory size.	10	CO2	L6																									

BLOOMS TAXANOMY LEVELS (BL)

1-REMEMBERING, 2-UNDERSTANDING, 3-APPLYING, 4-ANALYSING,
5-EVALUATING, 6-CREATING